APPARATUS AND METHOD FOR MINIMIZING SPURIOUS HARMONIC NOISE IN SWITCHED CURRENT STEERING ARCHITECTURES

RELATED APPLICATIONS

5   **[1]**   This application claims priority to U.S. Provisional Patent Application Serial No. 60/293,445, entitled "A Method for Reducing the Spurious Outputs of High Speed Digital-to-Analog Converters," filed on May 24, 2001.

BACKGROUND OF THE INVENTION

10   Field of the Invention

[2]   The present invention relates to techniques for minimizing third order harmonic output signal spurs in architectures having switched current steering elements. More particularly, the present invention comprises an apparatus and method for minimizing harmonic output signal spurs via a set of dummy switches that selectively

15   operate in conjunction with a set of actual switches.

Description of the Background Art

[3]   An ideal or hypothetical electrical system or circuit may operate upon a set of input signals to generate one or more corresponding output signals having intended or pure spectral content. Real-world electrical systems or circuits, however, produce or

20   generate noise components that may corrupt, interfere with, or distort a desired output signal frequency or frequency band.

[4]   Harmonic noise components arise from electrical mixing of frequencies, which causes difference and sum frequencies to appear in an output signal. Such

25   electrical mixing may involve one or more input signal frequencies, as well as one or more frequencies associated with internal circuit operation. Third order harmonic noise components are commonly believed to arise from distortion mechanisms caused by circuit non-linearity. However, third order harmonic noise components may alternatively or additionally imply a dependence upon the states of one or more input signals.

[5]   A variety of systems and circuits, such as Digital to Analog Converters (DACs), may include switches that control current steering elements. The current steering elements direct electrical current from one output to another. In a current steering DAC, timing mismatch between activated switches, as well as variations in

5   switch operation or activation sequences as a function of changes in input data over time, contribute to the generation of harmonic output signal noise components.

[6]   As input signal frequency, and hence switching frequency, increases, harmonic output signal noise undesirably increases, and Spurious Free Dynamic Range (SFDR) correspondingly degrades. One approach toward minimizing or controlling

10   spurious harmonic output signal noise is through the use of a sample and hold architecture. In a sample and hold architecture, circuit outputs are temporarily disconnected from output signal generating elements at the time at which switching is to occur. After a predetermined settling time has elapsed, the circuit outputs are reconnected to the output signal generating elements, whereupon output signals may

15   be delivered or transmitted. Unfortunately, to ensure error free operation, sample and hold circuitry must operate at twice the speed of the output signal generating elements. This constraint becomes significantly more difficult to meet at higher frequencies.

[7]   Another approach toward minimizing harmonic output signal noise is commonly referred to as dynamic element matching. In dynamic element matching,

20   pseudo-random bit sequences selectively determine whether particular switches that were in an on state during a most-recent output signal generation cycle, and which would normally remain in an on state during a next output signal generation cycle, shall be turned off between output signal generation cycles. This results in an averaging of harmonic output signal noise components because different numbers of switches are

25   activated during each output signal generation cycle. Unfortunately, dynamic element matching also results in an increase in a circuit's noise floor, which reduces the circuit's dynamic range.

SUMMARY OF THE INVENTION

[8]   In one embodiment, the present invention comprises a set of activation modules coupled to a set of switch modules. A switch module may comprise an actual driver coupled to an actual switch; and a dummy driver coupled to a dummy switch. An

5   activation module may comprise an actual signal latch, a dummy signal latch, and dummy signal logic.

[9]   An activation module may receive signals or bits corresponding to or derived from an incoming signal or data stream, where such incoming signals specify or indicate a next actual state associated with an actual switch. Based upon the current

10   state of an actual switch, the next state of the actual switch, and the current state of a dummy switch associated therewith, the activation module may selectively generate a dummy signal or bit to cause the dummy switch to experience a state transition. In particular, if the current and next states of the actual switch are identical, the dummy signal causes the dummy switch to undergo a state transition. If the current and next

15   states of the actual switch differ, the dummy switch is maintained in its current state.

[10]   Taken across multiple switch modules, the present invention may ensure that the total number of switches (i.e., actual switches and dummy switches taken together) that experience state transitions at any given time remains constant. As a result, the present invention may greatly reduce or essentially eliminate a major or

20   dominant contribution to third order spurious harmonic noise.

BRIEF DESCRIPTION OF THE DRAWINGS

[11]   FIG. 1 is a block diagram of an apparatus for minimizing spurious harmonic noise in switched current steering architectures according to an embodiment

25   of the invention.

[12]   FIG. 2 is a block diagram of a switch module according to an embodiment of the invention.

[13]   FIG. 3 is a circuit diagram of a activation module according to an embodiment of the invention.

[14]   FIG. 4 is a floorplan diagram of a Digital to Analog Converter that incorporates an embodiment of the invention.

[15]   FIG. 5 is a block diagram of a broadband upconversion system constructed in accordance with an embodiment of the invention.

[16]   Table 1 is a truth table corresponding to logic shown in FIG. 3.

DETAILED DESCRIPTION

[17]   FIG. 1 is a block diagram of an apparatus 100 for minimizing spurious harmonic noise in switched current steering architectures according to an embodiment of the invention. In one embodiment, the apparatus 100 comprises a switching unit 102 coupled to a switch activation unit 200. The switching unit 102 may include a set of switch modules 110, each of which is coupled to a corresponding activation module 210 within the switch activation unit 200. Each switch module 110 may comprise an actual switch driver 120, an actual switch 130, a dummy switch driver 140, and a dummy switch 150.

[18]   The switch activation unit 200 receives an input signal or data stream S, which in one embodiment comprises actual data signals or bits D_a and their complements. Particular actual data bits and/or their complements may be directed toward particular switch modules 110. As described in detail below, the switch activation unit 200 selectively generates dummy data signals or bits D_d, and outputs or delivers actual data signals and dummy data signals to actual and dummy switches 130, 150, respectively.

[19]   The present invention may minimize or eliminate third order harmonic noise components arising from digital switching transients by providing a constant, essentially constant, or well controlled switching noise environment. In one embodiment, the switch activation unit 200 selectively activates an actual switch 130 or a dummy switch 150 within each switch module 110 in the apparatus 100 during any given switching cycle. As a result, the total number of switches undergoing state transitions from one switching cycle to another remains constant. The present invention eliminates variations in switch activation sequences as a function of input signal

4

changes over time, thereby eliminating a major or dominant contribution to third order harmonic noise. The present invention may be particularly advantageous or useful in applications such as digital radio, cellular telephony, wireless communications, or waveform generation.

5 **[20]** FIG. 2 is a block diagram of a switch module 110 according to an embodiment of the invention. The actual switch 130 may comprise a current steering element, in a manner readily understood by those skilled in the art. The actual switch 130 may be coupled to a first current source 180, and may provide or generate a first and a second actual output signal. An actual switch 130 may be conventional, having a

10 structure analogous or identical to a current steering element within a conventional Digital to Analog Converter (DAC), for example. The actual switch driver 120 may comprise circuitry for driving the current steering element to which it is coupled, and may be conventional.

[21] The dummy switch 150 may comprise a current steering element, and the

15 dummy switch driver 140 may comprise circuitry for driving the current steering element to which it is coupled. The dummy switch 150 may be coupled to a second current source 190, and may provide or generate a first and a second dummy output signal in a manner analogous to that for the actual switch 130.

[22] In one embodiment, the first and second current sources 180, 190 provide

20 different levels of electrical current to the actual and dummy switch 130, 150, respectively. The actual switch 130 and the dummy switch 150, however, may provide or correspond to an identical or essentially identical electrical load.

[23] The dummy switch driver 140 and the dummy switch 150 may be structurally analogous or identical to an actual switch driver 120 and an actual switch

25 130, respectively. In one embodiment, the present invention includes a dummy switch 150 corresponding to each actual switch 130. An exemplary embodiment of the present invention may include twenty five switch modules 110, thereby providing or incorporating twenty five actual switches 130 and twenty five corresponding dummy switches 150. In such an embodiment, the second current source 190 may provide a

current that is less than that provided by the first current source 180 by approximately an order of magnitude.

[24]	In one embodiment, an actual switch driver 120 is coupled to receive an actual data bit D_a and its complement from the switch activation unit 200. The actual switch driver 120 drives the actual switch 130 in accordance with the actual data bit and its complement, in a manner readily understood by those skilled in the art.

[25]	A dummy switch driver 140 may be coupled to receive a dummy data bit D_d and its complement from the switch activation unit 200. The dummy switch driver 140 may drive the dummy switch 150 in accordance with the dummy bit and its complement, in a manner readily understood by those skilled in the art.

[26]	FIG. 3 is a circuit diagram of an activation module 210 according to an embodiment of the invention. In one embodiment, the activation module 210 comprises an actual signal latch or flip-flop 220, a dummy signal latch or flip-flop 240, and dummy signal logic 250. The actual signal latch 220 and the dummy signal logic 250 are coupled to receive input signals from, corresponding to, or specified in accordance with the input signal stream S. In particular, the actual signal latch 220 and the dummy signal logic 250 may be coupled receive an actual bit D_a and its complement, where the actual bit D_a corresponds to a particular bit position and/or power of two within the input data stream S. The dummy signal logic 250 is coupled to deliver one or more dummy signals or bits to the dummy signal latch 240. The actual signal latch 220 and the dummy signal latch 240 are coupled to an actual switch driver 120 and a dummy switch driver 140, respectively, within a corresponding switch module 110. Additionally, the dummy signal logic 250 is coupled to outputs of the actual and dummy signal latches 220, 240.

[27]	Input signals received by an activation module 210 may be defined or designated as specifying a next actual state (NAS), indicating a next state for the actual switch 130 coupled to the activation module 210. Signals currently output by the actual signal latch 220 may be defined as specifying a present actual state (PAS), indicating a present or current state for the actual switch 130 coupled to the activation module 210. Similarly, signals generated or output by the dummy signal logic 250 may be defined as

specifying a next dummy state (NDS), indicating a next state for a dummy switch 150 coupled to the activation module 210. Finally, signals currently output by the dummy signal latch 240 may be defined as specifying a present dummy state (PDS), indicating a present or current state for the dummy switch 150 coupled to the activation module

5   210.

[28]   Table 1 is a truth table corresponding to the dummy signal logic 250 of FIG. 3. Present and next states associated with an actual and a dummy switch 130, 150 are defined in the manner described above. The dummy signal logic 250 may operate in accordance with the truth table to generate a dummy data signal, such as a

10   dummy data bit D_d and its complement. Via the dummy signal latch 240, the dummy data bit D_d and its complement may be delivered or issued to a dummy switch 150 during a next switching cycle. The dummy signal latch 240 may deliver the dummy signal to a dummy switch 150 in conjunction with the actual signal latch 220 delivering an actual signal to an actual switch 130.

15

Actual Switches   Dummy Switches

NAS	CAS	CDS	NDS
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Table 1

20   **[29]**   In the event that a next actual state differs from a current actual state associated with an actual switch 130, the dummy signal logic 250 may ensure that the state of a corresponding dummy switch 150 remains unchanged. In the event that a next actual state is identical to a current actual state associated with an actual switch

7

130, the dummy signal logic 250 may ensure that dummy switch 150 associated with the actual switch undergoes a switching transition.

[30]   The dummy logic 250 may therefore selectively cause a dummy switch 150 coupled thereto to undergo a switching transition when the state of an actual switch

5   130 corresponding to or associated with the dummy switch 150 will remain unchanged from a present switching cycle to a next switching cycle. The present invention may thereby ensure that the total number of actual and dummy switches 130, 150 that experience switching transitions in any given switching cycle remains constant across the switching modules 110. As a result, switching power and noise profile may remain

10   constant or essentially constant from one switching cycle to another.

[31]   FIG. 4 is an architectural floorplan of a Digital to Analog Converter 300 according to an embodiment of the invention. Within the DAC 300, a switch activation unit 200 corresponds to and/or resides within a digital portion of the DAC 300, while a switching unit 102 corresponds to and/or resides within an analog portion of the DAC

15   300, in a manner readily understood by those skilled in the art.

[32]   FIG. 5 is a block diagram of a broadband upconversion system 400 according to an embodiment of the invention. In one embodiment, the broadband upconversion system 400 comprises a programmable upconversion stage 410, an interpolation stage 420, a DAC 300, a bandpass stage 430, a local oscillator mixing

20   stage 440, a power amplification stage 450, and an antenna 460.

[33]   The programmable upconversion stage 410 may filter and upconvert baseband data to intermediate bandpass data in accordance with one or more programmable channels. The interpolation stage 420 may increase a sample rate of the bandpass data by an integer factor, and may also upconvert the intermediate

25   bandpass data to a second intermediate frequency. The bandpass stage 430 may filter the second intermediate frequency signal output by the DAC 300. The local oscillator mixing stage 440 may upconvert the second intermediate frequency signal to a desired radio frequency. The power amplification stage 450 may amplify the radio frequency signal to a sufficient power level for transmission through a medium. Finally, the

antenna 460 may transmit the radio frequency signal in the form of an electromagnetic radio wave.

[34]   The general principles described herein may be applied to embodiments and applications other than those detailed above without departing from the spirit and scope of the present invention as defined by the appended claims. As an example, a switched current steering architecture may include a number of dummy switches that is different from a number of actual switches. The present invention is to be accorded the widest scope consistent with the principles and features disclosed herein, and is limited only by the following claims: